![ASIC logo]

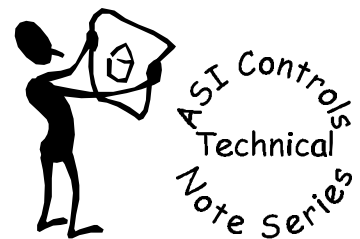# New Combined Firmware for ASIC/2-7040C and ASIC/2-8040 Controllers.

Effects: ASIC/1-8040, ASIC/1-7040C
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ASI Controls Technical Note Series

Note No. TE004

Notification of New Firmware

The latest versions of ASIC/2-7040C Ver 2.0 and ASIC/2-8040C 1.0 are about to be released.

They offer some significant enhancements and changes to previous versions.

- The new firmware uses the same source code in development for the first time. This may seem an obscure feature but it means that when additions are made to Objects, they will be available in both products simultaneously. This will mean that the products will grow together rather than with version difference between models.

It does not mean that firmware chips are interchangeable!

ASIC/2-8040 Changes

This makes some fundamental enhancements to the ASIC/2-8040. For the first time this product will include:

- DAK support is included.
- Dial Manager is available - The RS232 connection is fixed to the System Bus used for dialing.
- Calendar Object and Special days
- Encoder Object
- Linear Input conversion in Input Object
- Names for certain Objects
- Compensated Temperature Sensor Conversions added to Input Object

Changes to Object Operation

Object 5 - Input Object (7040C/8040C)

Additional thermistor temperature conversions are now built into the Input Object. Two sets exist with and without self-heating compensation. Self Heated compensated should be used for room sensors. For duct, immersion and outside sensors we suggest non-compensated conversion.

Object 12 - Clock Object (7040C/8040C)

This is an important change to controller operation - please read carefully!

We have made changes to the relationship between the hardware clock and the software clock. In all controllers the software clock has always been the keeper of time in the controller, the hardware clock (if enabled) only synchronized the software clock every minute at the minute change. Since many operations also happen at the minute, such as schedules etc it is a very busy transition time.

We have modified this relationship in the following way.

- Hardware Clock Enable is redefined as Time Keeper Enable.
- The internal operation of the controller is based on the software clock.
- The Time Keeper will read the hardware clock once an hour at a time which represents an odd number of minutes that does not conflict with any controller events.
- If the controller is not a Time Keeper the hardware clock is only read at power up as a back up. This is a significant change. Now when a controller in software clock mode is reset it will synchronize itself from its own clock chip.

With this version the Timekeeper's Hardware Clock is always updated whenever there is a 3FH, M1=1 message. The Timekeeper ignores the update enable and is always synchronized. Only the Time Keeper may Broadcast Time, 3Fh,M1-1 or 38h on the system bus. Broadcast of Time will work in both token and non-token mode. (Non-Token Enable is not needed.)

For others the Update Enable should always be set so that the hardware clock can be updated. (In older versions Update Enable should always be set so that the Time Keeper can be updated.)

The recommended set up for a network of controllers incorporating the new release firmware is to have one Timekeeper enabled. Other controllers should be set to software clock (Timekeeper or Hardware Clock not enabled.) These controllers will receive time broadcasts on the system bus for synchronization. If they lose power their own local hardware clock will synch the time.

You may set all ASIC/2 to Timekeeper (Hardware Clock) Enable if the communication system cannot be relied on to ensure system synchronization. However, the best performance of clock, communications, and time related functions occurs when the Time Keeper Function is not enabled since the time-intensive function of synching software clock to hardware clock is removed from the microprocessor.

If multiple TimeKeeper/ Hardware Clocks are enabled, Make sure that only one device is the synchronizing device broadcasting the time. If more than one device sends time synchronizations, unexpected results will occur.

The Calendar must reside in the device that synchronizes the time since the Special Days are broadcast as part of the time message.

Object 4 - Schedule Changes

At the release of the ASIC/2-7040C (1/97) we modified the operation of the Time Schedules:

Originally a setting of zero hours meant not used. This was changed to the following

- IF On-time=0 and Off-time <> 0; then schedule is Always Off.
- IF On-time=0 and Off-time = 0; then schedule is Always Off.
- IF On-time = Off-time ; then schedule is Always Off.
- IF On-time<>0 and Off-time 0; then schedule is Always On.

If both the Off-time and On-time are non-zero,
then the schedule is active and its output depends On comparing the
On and Off-times with the current time in the controller.

The latest versions of both ASIC/2-7040 and ASIC/2-8040 include a new flag **Use Old Schedule** option to Schedule object, SCH,Attr-11,LO bit 7 .If Use Old Schedule is set it works as it did in earlier product providing backward compatibility with earlier models. Download a new Setsys to obtain scripts displaying this parameter.

Polling (Objects 13 and 17) ASIC2-7040C

With 740C ver2.0 the polling is modified to provide improved operation of certain functions.

Added protection for corrupt messages because of other traffic on the line. This prevents users connected to local bus controllers from temporarily corrupting the poll data within the Poll List because of collisions.

The polling error function in the Poll List is also modified. The polling will try only once to communicate with a device before moving to the next item. This significantly increases performance by not polling three times for unreachable devices.

Errors are counted differently. Before after three immediate attempts, an error was flagged. Now, after failed attempts in five successive rounds of polling the error flag is set. It clears immediately on a successful communication.

Changed Poll List Communications Error Counter
        Attr-5 LSNBL Comm Try Counter
        Attr-5 MSNBL Comm Fail Counter

The Comm Try Counter is incremented when ever there is an unsuccessful communication.
The Comm Try Counter is cleared when ever there is an successful communication.
If the Comm Try Counter reaches 5, then Attr-2 bit 5 Comm Error Status is set
the Comm Fail Counter is incremented, and the Comm Try Counter is cleared.
The Comm Error Status is cleared when ever there is an successful communication.

(Older Setsys Scripts displaying a single error counter will appear to count in a disjointed fashion)